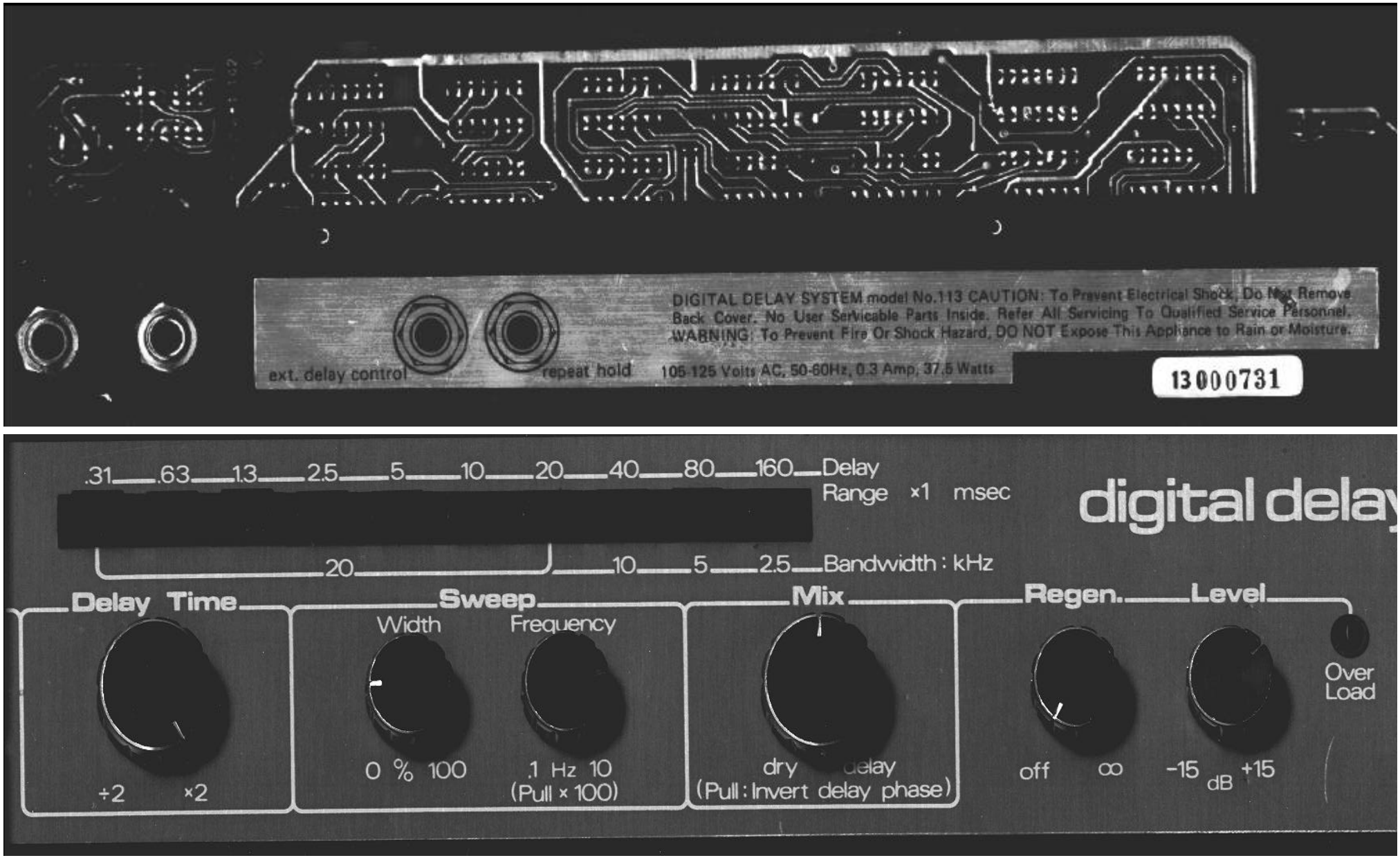
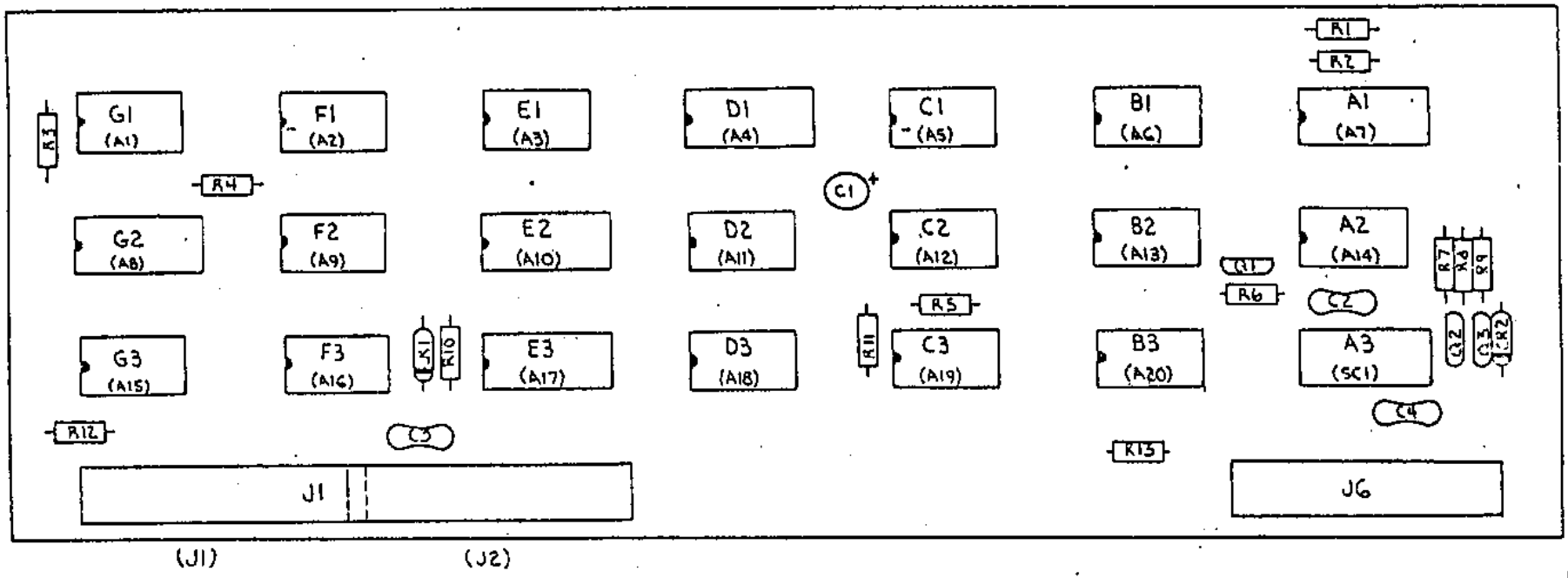
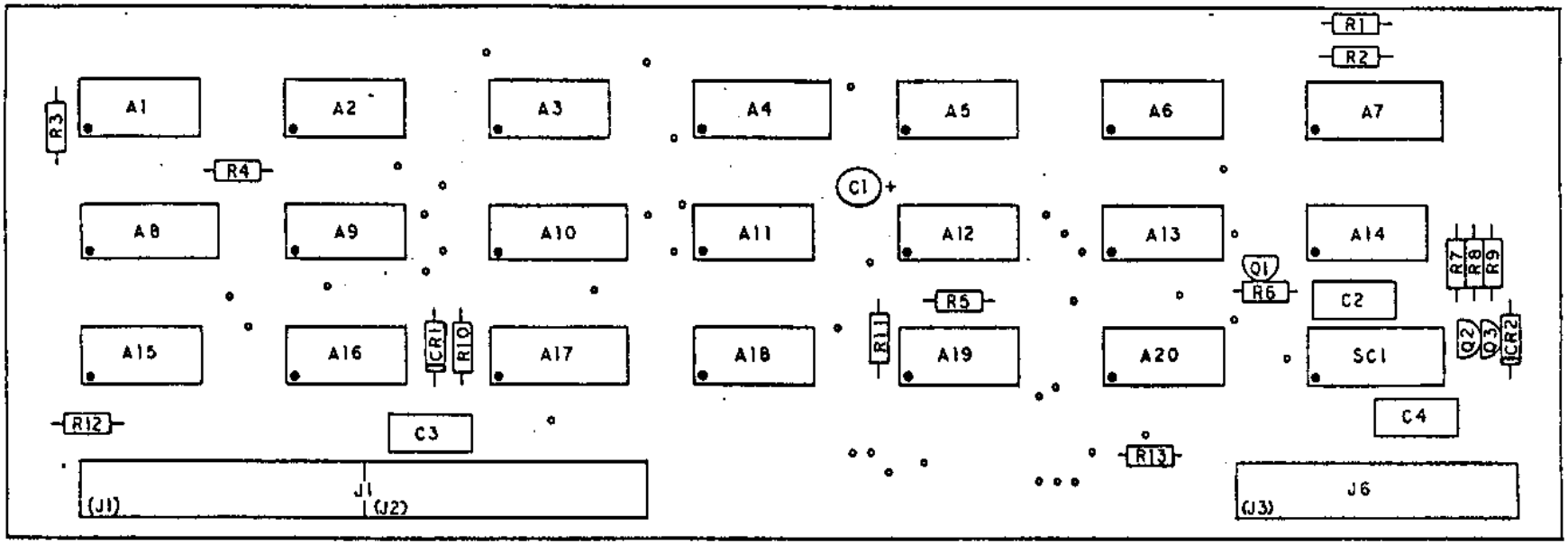

DIGITAL DELAY SYSTEM model No.113 CAUTION: To Prevent Electrical Shock, Do Not Remove Back Cover. No User Servicable Parts Inside. Refer All Servicing To Qualified Service Personnel.
WARNING: To Prevent Fire Or Shock Hazard, DO NOT Expose This Appliance to Rain or Moisture.
ext. delay control
repeat hold
105-125 Volts AC, 50-60Hz, 0.3 Amp, 37.5 Watts
13000731
.31 .63 1.3 2.5 5 10 20 40 80 160 Delay Range ×1 msec
digital delay
20 10 5 2.5 Bandwidth : kHz
Delay Time
÷2 ×2
Sweep
Width
Frequency
0 % 100
.1 Hz 10
(Pull × 100)
Mix
dry delay
(Pull : Invert delay phase)
Regen.
off ∞
Level
-15 dB +15
Over Load



VIEW OF COMPONENT SIDE OF BOARD

P.C.B. NO. 113-3001-103

	MXR INNOVATIONS INC.		
ORIGINAL		SCALE 2:1	
FRACTIONAL —	TITLE COMPONENT PLACEMENT TTL BOARD - DIGITAL DELAY		
ANGULAR —	DATE 4-4-78	DRAWING NUMBER 113-3001-102	



NOTE:
USE LATEST REV OF 113-3001-100
LEVEL PER REV LOG.

VIEW of COMPONENT SIDE of BOARD

LEVEL	DATE	PEN NO. OR CHANGE REMARKS	DRAWN	APP'D
—	3/10/80	RECRAWN NO/CHG	H.H.H.	TH
302	11/6/78	REV COMP DESIGNATIONS	S.D.	S.D.

REVISION LOG

TOLERANCES: (UNLESS OTHERWISE NOTED)
DECIMAL: 2 Pl. ±, 3 Pl. ±
FRACTIONAL: ±
ANGULAR: ±

PRINT DATE:

MXR MXR Innovations Inc. Rochester, New York

SCALE: 2:1

DRAWN: T. BACKHART DATE 4/4/78

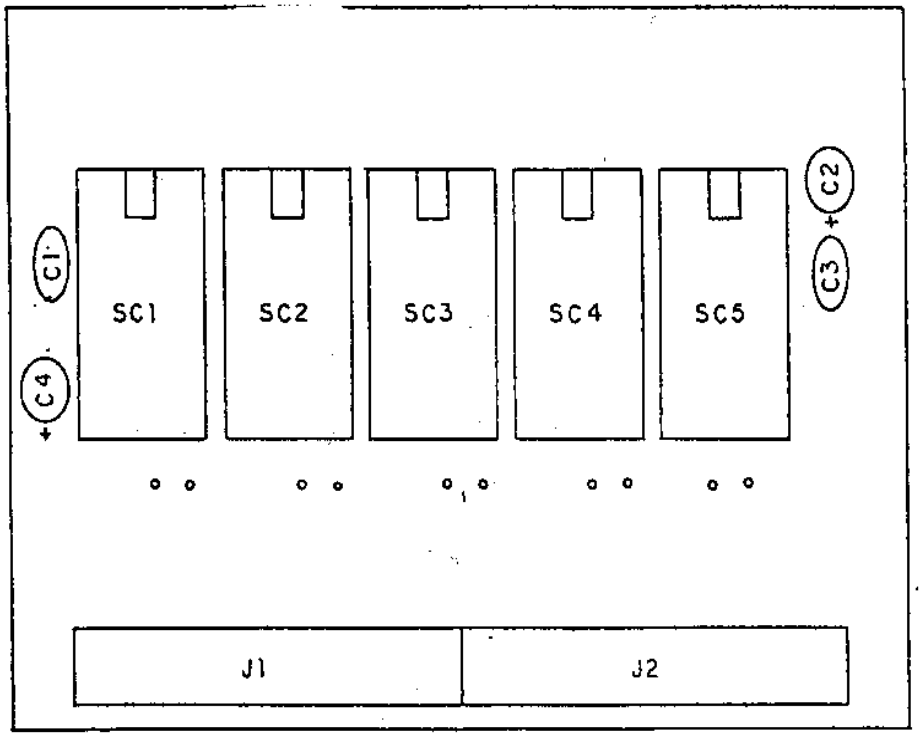
CHK'D: DATE

APP'D: D. TEAGUE DATE 4/4/78

TITLE: COMPONENT PLACEMENT
TTL BOARD-DIGITAL DELAY

DWG. NO. 113-3001

REV LEVEL 302



VIEW of COMPONENT SIDE of BOARD

NOTE:
USE LATEST REV OF 113-3002-100
LEVEL PER REV LOG.

LEVEL	DATE	PCN NO. OR CHANGE REMARKS	DRAWN	APP'D
—	3/7/80	REDRAWN W/O CHG	H.H.H.	
—	12/5/78	DELETED "A" ADDED "J"	B.K.	D.Y.

REVISION LOG

TOLERANCES: (EXCEPT AS NOTED)
DECIMAL:
1 PL.
2 PL.
FRACTIONAL:
ANGULAR:

PRINT DATE:

MXR Innovations Inc.
Rochester, New York

SCALE: 2:1
DO NOT SCALE DRAWING
DIMENSIONS ARE IN: ☐ INCHES ☐ M M

DRAWN: T. BANNART DATE 4/11/78
CHK'D: DATE
APP'D: D. YEAGER DATE 4/11/78

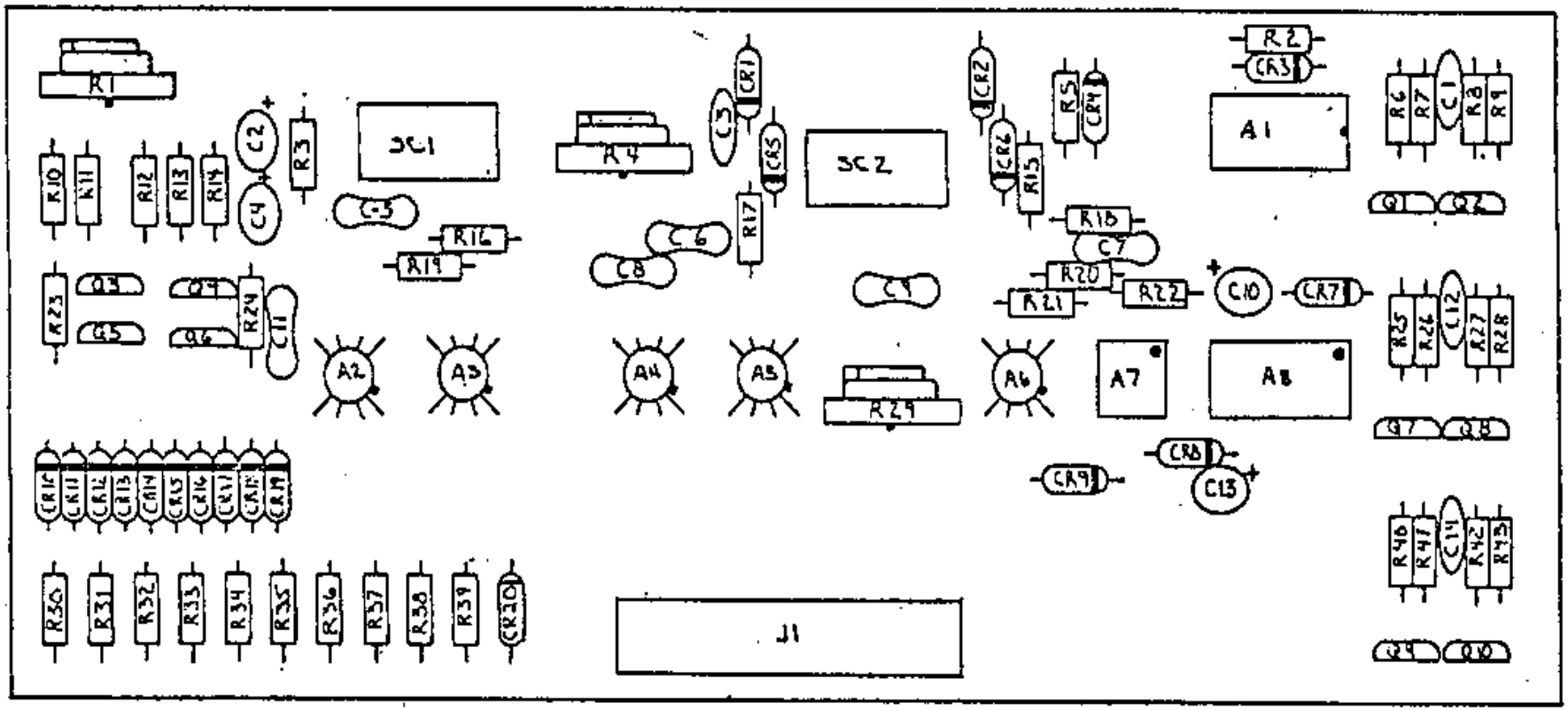
TITLE: COMPONENT PLACEMENT
MEMORY MODULE-DIGITAL DELAY

SHEET NO. OF

B

DWG. NO. 113-3002

REV. LEVEL 301

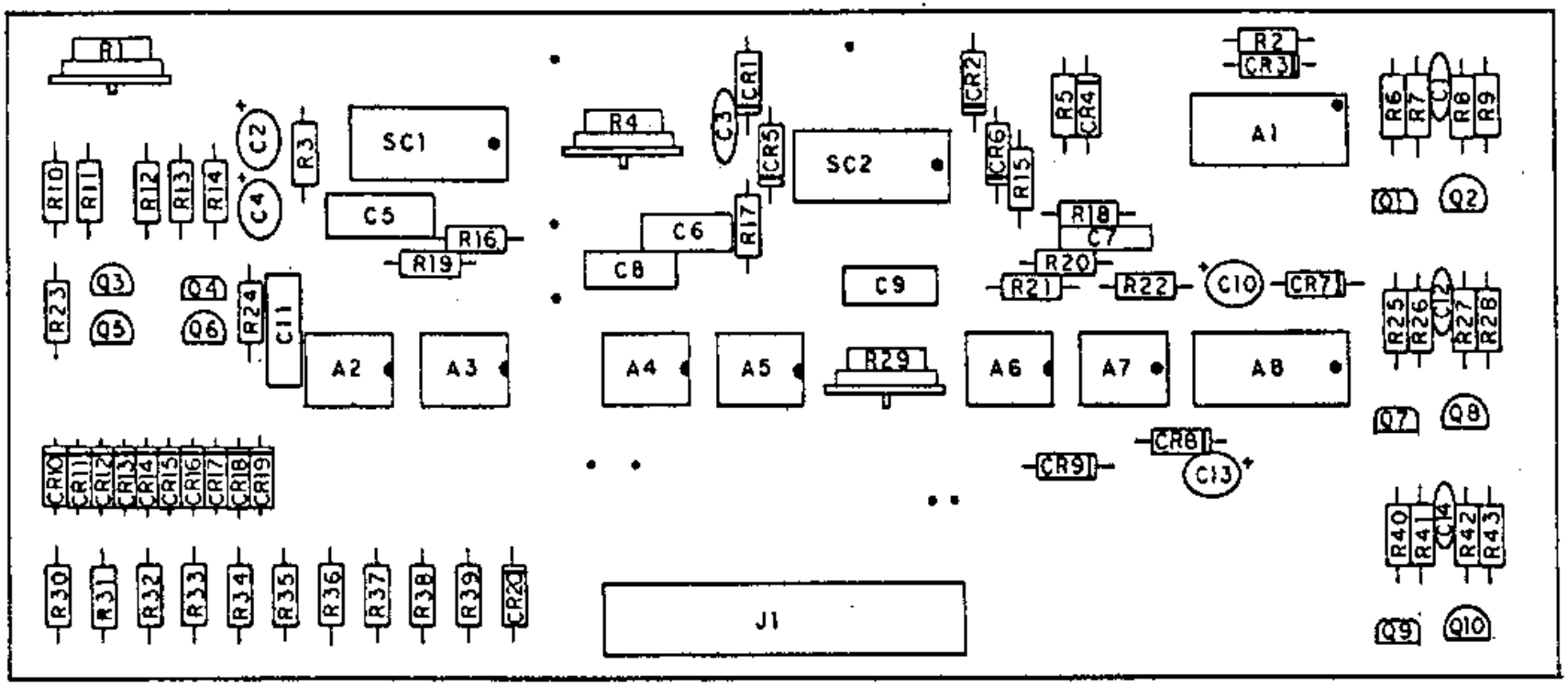


Analog Switching Board

VIEW OF COMPONENT SIDE OF BOARD

P.C.B. NO. 113-3003-103

TOLERANCES	MLR INNOVATIONS INC.	
		SIZE A11
	TITLE COMPONENT PLACEMENT ANALOG SWITCHING BOARD - DIGITAL DELAY	
	DATE 4-3-78	113-3003-302



VIEW of COMPONENT SIDE of BOARD

NOTE:
USE LATEST REV OF 113-3003-100
LEVEL PER REV LOG.

LEVEL	DATE	PCN NO. OR CHANGE REMARKS	DRAWN	APP'D
—	3/10/80	REDRAWN NO CHG	H.H.H.	
302	10/16/78	DELETE R18, R22 25.5K ADD R18, R22 22.6K	B.K.	J.L.

REVISION LOG

TOLERANCES: (EXCEPT AS NOTED)
DECIMAL:
2 PL.
3 PL.
FRACTIONAL:
ANGULAR:

PRINT DATE:

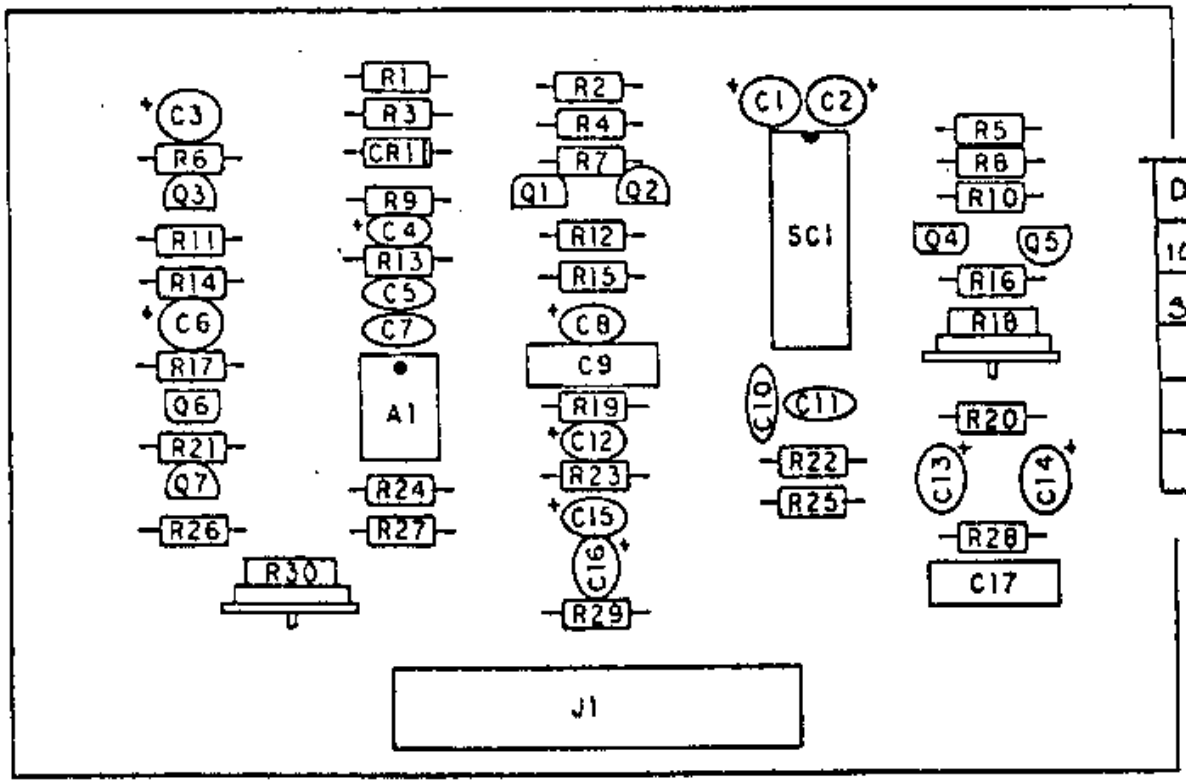
MXR
MXR Innovations Inc.
Rochester, New York

SCALE: 2:1
DO NOT SCALE DRAWING
DIMENSIONS ARE IN: INCHES / M.M.
DRAWN / CHECKED DATE 4/3/78
APPROVED DATE 4/3/78

TITLE: COMPONENT PLACEMENT
ANALOG SWITCHING BOARD
DIGITAL DELAY

DWG. NO. 113-3003
REV LEVEL 302

PG OF



VIEW of COMPONENT SIDE of BOARD

NOTE:
USE LATEST REV OF 113-3004-100
LEVEL PER REV LOG.

PARTS LIST

ITEM	DESCRIPTION	PART NO.	QTY.

DATE	SYM.	REVISION	APP'D	DRN	CHK.
10-12-78		C12 15MF → 47MF	DY	[illegible]	[illegible]
3-6-79	C-10,11	See PPCO 104	TL	[illegible]	[illegible]

LEVEL	DATE	PCN NO. OR CHANGE REMARKS	DRAWN	APP'D
—	3/11/80	REDRAWN W/CHG	H.H.H.	[illegible]
303	3/6/79	PPCO 104		
302	10/12/78	DELETED C12 15 MF ADDED C12 47MF	B.K.	D.Y.

REVISION LOG

TOLERANCES: (UNLESS OTHERWISE NOTED) DECIMAL: ±.XX ±.XXX FRACTIONAL: ANGULAR:

PRINT DATE:

MXR Innovations Inc. Rochester, New York

SCALE: 2:1

DRAWN: T. BACKHAUS DATE: 6/7/78

CHK'D: [illegible] DATE: 7/11/78

APP'D: D. YEAGER DATE: 6/7/78

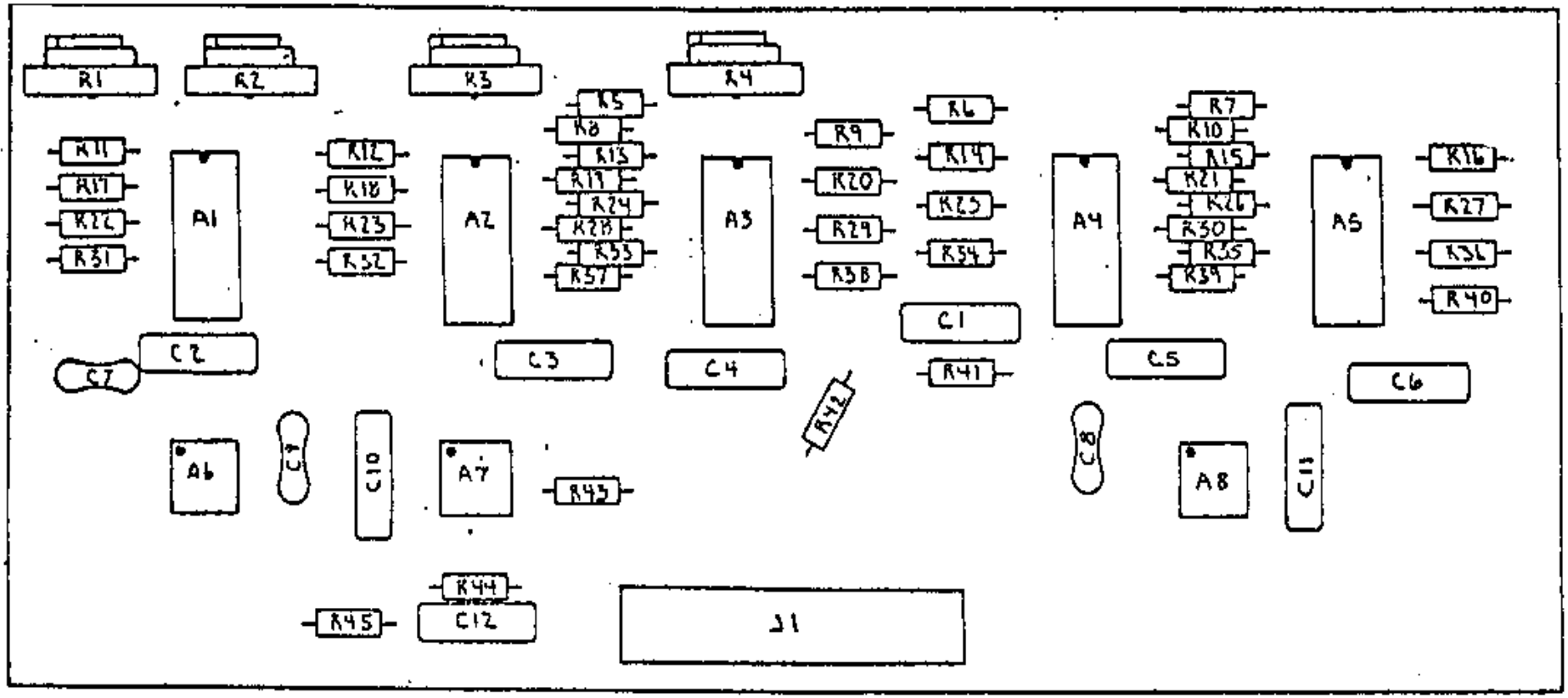
TITLE: COMPONENT PLACEMENT
COMPANDER BOARD-DIGITAL DELAY

SIZE: B

DWG. NO. 113-3004

REV. LEVEL 303

PG OF

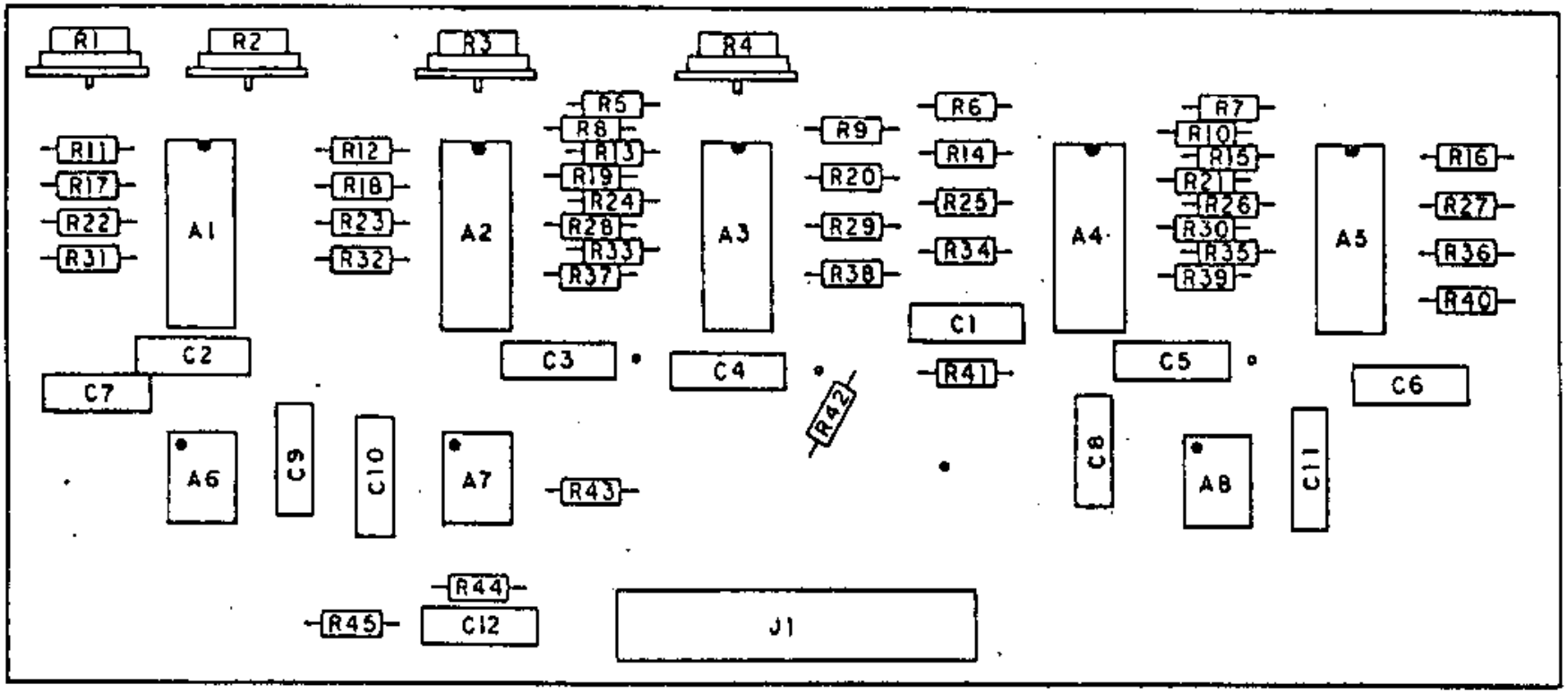


Filter Board

VIEW OF COMPONENT SIDE OF BOARD

P.C.B. NO. 113-3005-103

TOLERANCES UNLESS OTHERWISE SPECIFIED	MKR INNOVATIONS INC.		
DECIMAL .x ± .03		SCALE 2:1	DRAWN BY
FRACTIONAL ± 1/64	TITLE FILTER BOARD - COMPONENT LOCATION		
ANGULAR ± 1°	DATE 4-11-78	DRAWING NUMBER 113-3005-501	



VIEW of COMPONENT SIDE of BOARD

NOTE:
USE LATEST REV OF 113-3005-10C
LEVEL PER REV LOG.

LEVEL	DATE	PCN NO. OR CHANGE REMARKS	DRAWN	APP'D
—	3/11/80	REDRAWN W/O CHG	H.H.H.	

REVISION LOG

TOLERANCES: (EXCEPT AS NOTED)
DECIMAL: 2 PL. ±.01, 3 PL. ±.005
FRACTIONAL:
ANGULAR:

PRINT DATE:

MXR Innovations Inc. Rochester, New York

SCALE: 2:1

DRAWN: [illegible] 4/11/78

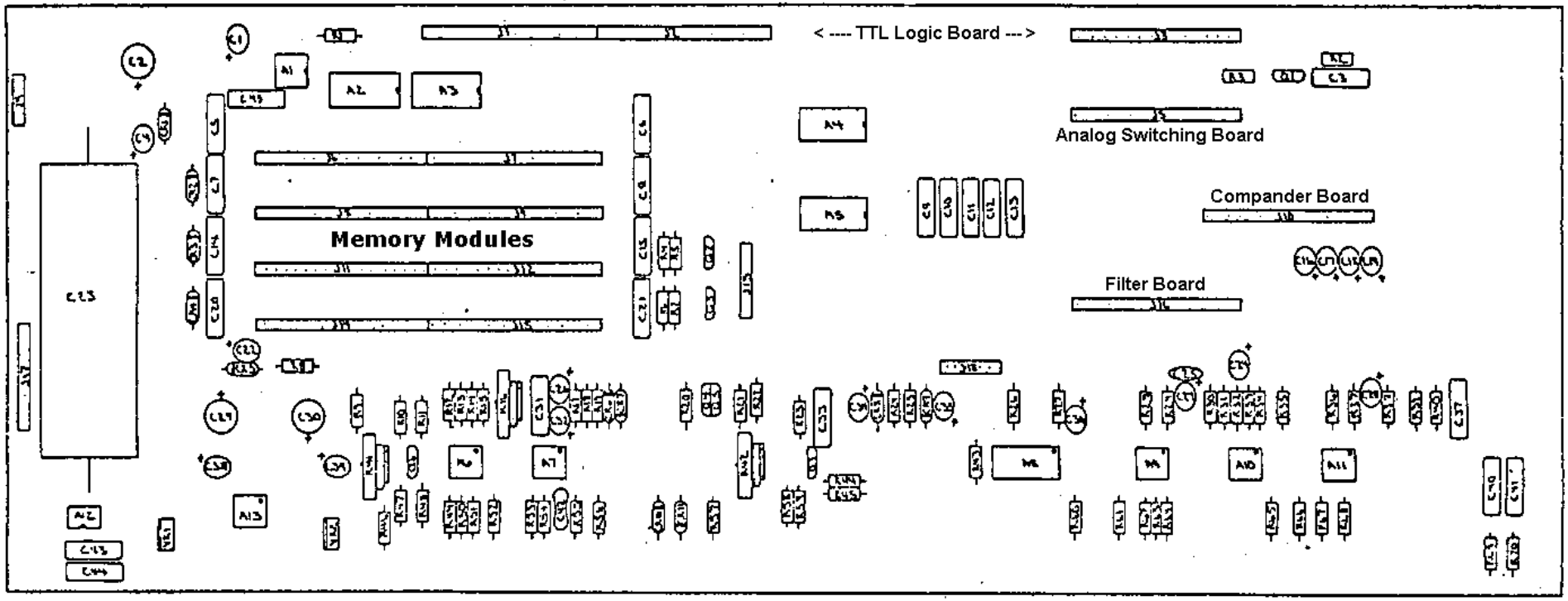
CHK'D: [illegible]

APP'D: D. TEAGUE 4/11/78

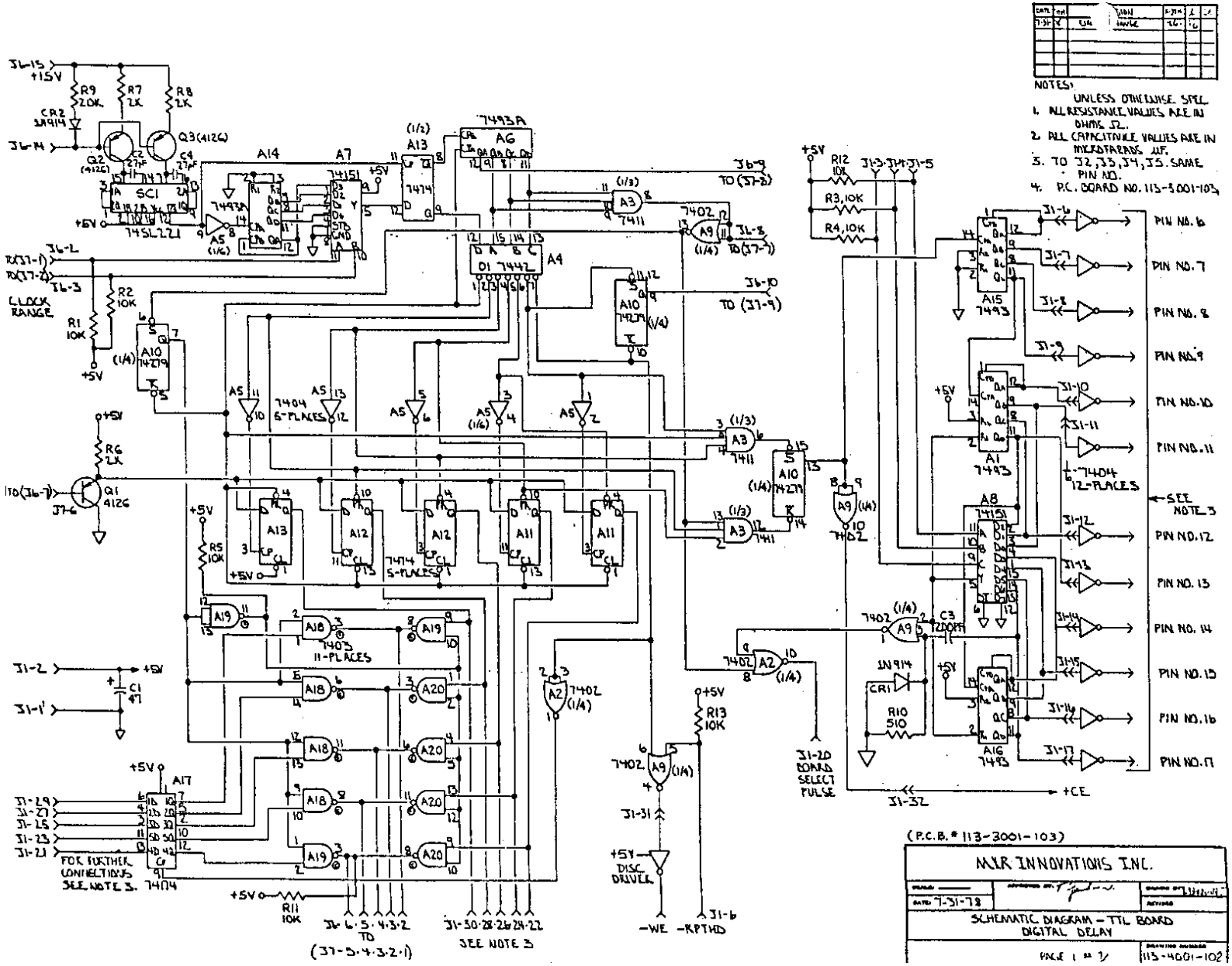
TITLE: COMPONENT PLACEMENT
FILTER BOAD DIGITAL DELAY

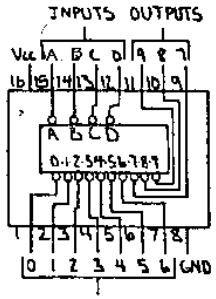
DWG. NO. 113-3005

REV LEVEL 30[illegible]

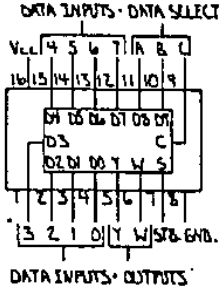

< ---- TTL Logic Board --- >
Analog Switching Board
Compander Board
Filter Board
Memory Modules

Main Board

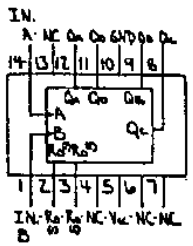

NOTES:
UNLESS OTHERWISE SPEC.
1. ALL RESISTANCE VALUES ARE IN OHMS Ω.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS μF.
3. TO J2,J3,J4,J5 SAME PIN NO.
4. P.C. BOARD NO. 113-3001-103
J6-15 +15V
R9 2.0K
R7 2K
R8 1K
CR2 1N914
J6-14
Q3(4126)
Q2 (4126)
C2 27pF
C4 27pF
SCI
74SL221
A14
A7
74151
74153A
A5 (1/6)
(1/2) A13
7474
7493A
AG
J6-9
TO (J7-8)
A3 7411
7402
A9 (1/4)
J6-8
TO (J7-7)
J6-L
R(J7-1)
R(J7-2)
J6-3
CLOCK RANGE
R1 10K
R2 10K
A10 74279 (1/4)
A4
D1 7442
A10 74279 (1/4)
J6-10
TO (J7-9)
7404 6-PLACES
A5 (1/6)
+5V
R6 2K
TO(J6-7)
Q1 4126
J7-6
A13
A12
A11
7474 5-PLACES
A3 7411 (1/3)
A10 74279 (1/4)
A9 (1/4) 7402
R5 10K
A19
A18
7403 11-PLACES
A20
A2 7402 (1/4)
J1-2
J1-1
C1 47
A17
J1-29
J1-27
J1-25
J1-23
J1-21
FOR FURTHER CONNECTIONS SEE NOTE 3. 74174
R11 10K
J6-4·5·4·3·2 TO (J7-5·4·3·2·1)
J1-30·28·26·24·22 SEE NOTE 3
R13 10K
7402 A9 (1/4)
J1-31
+5V DISC DRIVER
-WE -RPTHD
J1-6
R12 10K
J1-3·J1-4·J1-5
R3, 10K
R4, 10K
A15 7493
A1 7493
A8 74151
A16 7493
PIN NO. 6
PIN NO. 7
PIN NO. 8
PIN NO. 9
PIN NO. 10
PIN NO. 11
7404 12-PLACES
SEE NOTE 3
PIN NO. 12
PIN NO. 13
PIN NO. 14
PIN NO. 15
PIN NO. 16
PIN NO. 17
C3 120PF
1N914 CR1
R10 510
J1-20 BOARD SELECT PULSE
J1-32
+CE
(P.C.B.# 113-3001-103)
MLR INNOVATIONS INC.
7-31-78
SCHEMATIC DIAGRAM - TTL BOARD
DIGITAL DELAY
PAGE 1 OF 2
115-4001-102



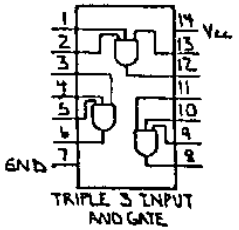
OUTPUTS
DECADE DECODER
7442



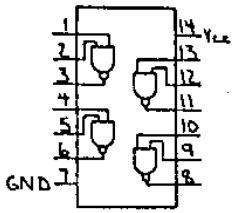
DATA INPUTS · OUTPUTS
8 INPUT MULTIPLEXER
74151



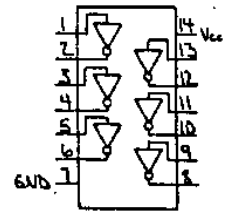
4 BIT COUNTER
7493



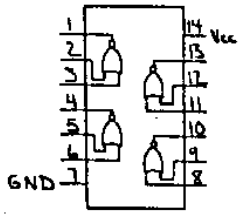
TRIPLE 3 INPUT
AND GATE
7411



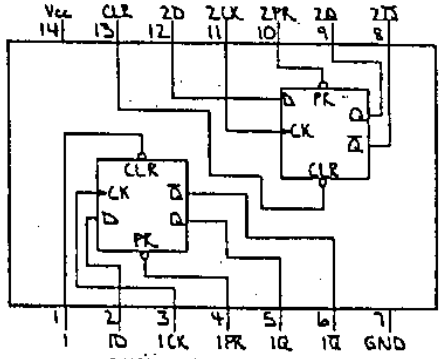
QUAD NAND GATE
7400
7403



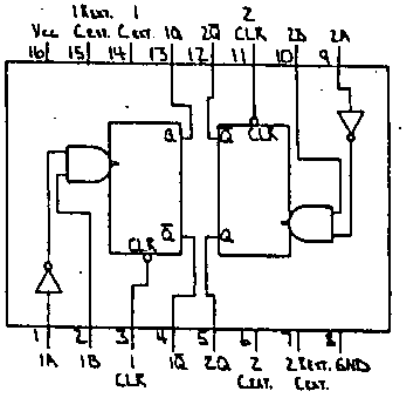
HEX INVERTER
7404



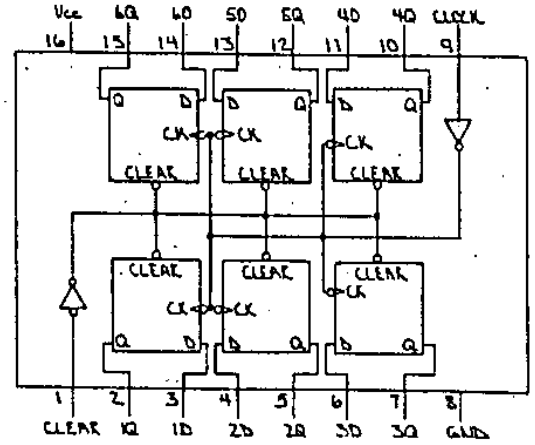
QUAD AND GATE
7402



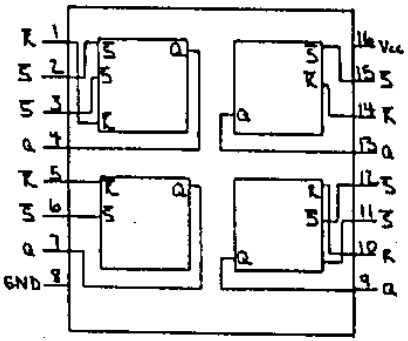
DUAL D-TYPE FLIP FLOP
7474



DUAL ONE-SHOT
74221

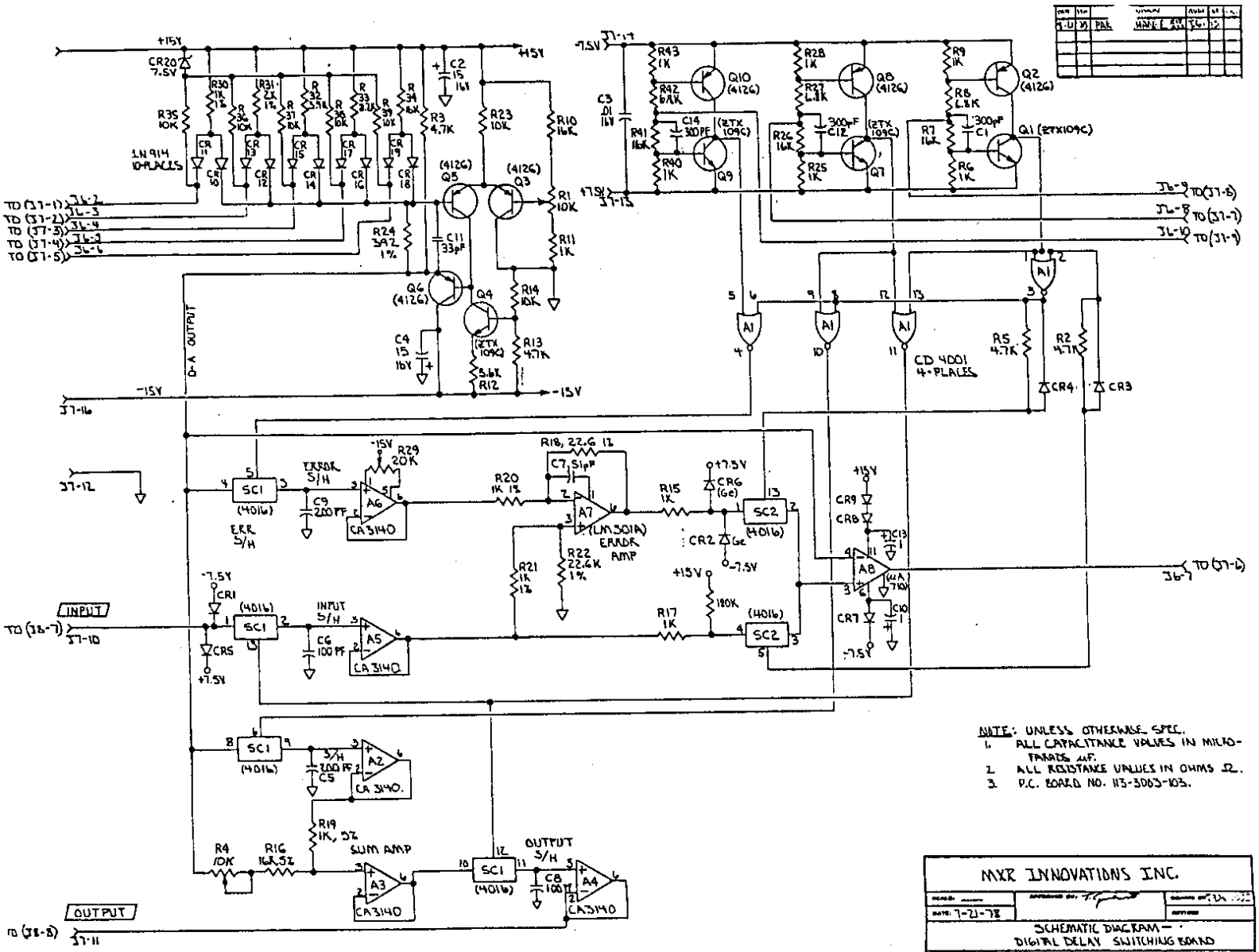


HEX D-TYPE LATCH
74174



QUAD R-S FLIP FLOP
74279

MXR INNOVATIONS INC.		
DATE 8-29-78	APPROVED BY: T. Jurmann	DRAWN BY: Wilson-T
COMPONENT PIN OUT – SCHEMATIC TTL BOARD – DIGITAL DELAY		
PAGE 1 OF 2		113-4001-102



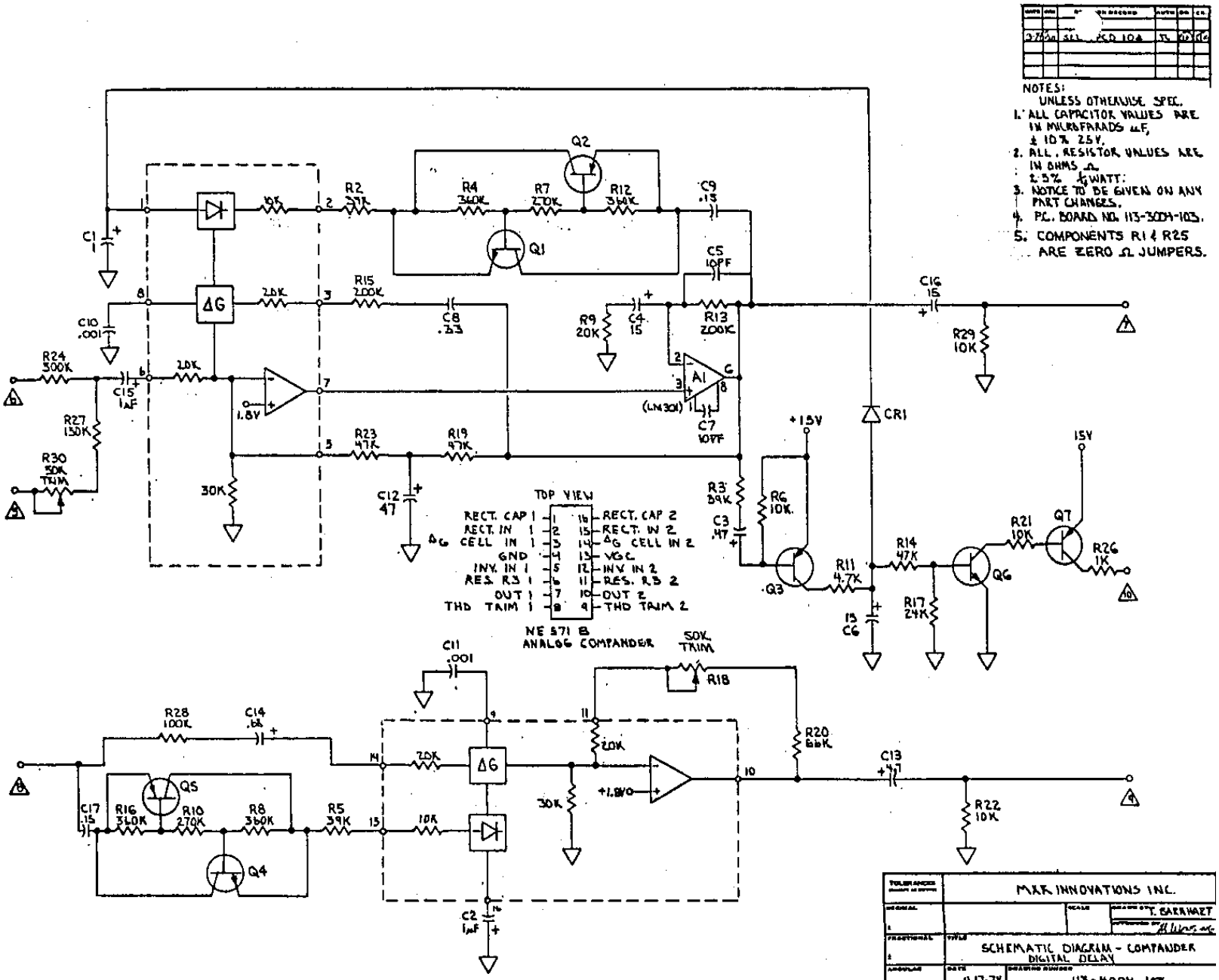
NOTE: UNLESS OTHERWISE SPEC.
1. ALL CAPACITANCE VALUES IN MICRO-FARADS, μF.
2. ALL RESISTANCE VALUES IN OHMS Ω.
3. P.C. BOARD NO. 113-3003-103.

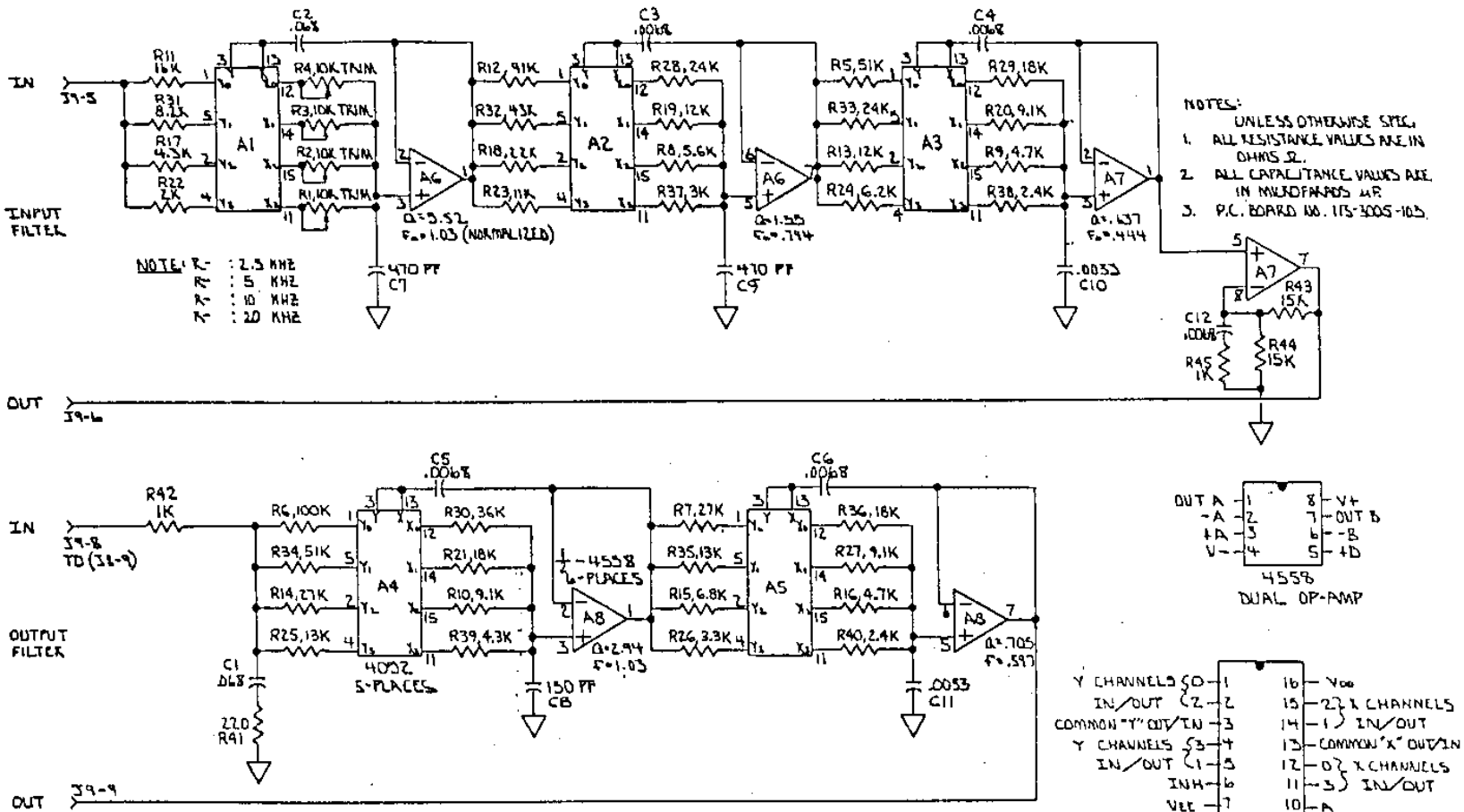
MXR INNOVATIONS INC.

DRAWN	APPROVED BY	DRAWING NO.
DATE 7-21-78		REVISED

SCHEMATIC DIAGRAM — DIGITAL DELAY SWITCHING BOARD

REGISTERED NUMBER 113-4003-102


NOTES:
UNLESS OTHERWISE SPEC.
1. ALL CAPACITOR VALUES ARE IN MICROFARADS μF, ± 10% 25V.
2. ALL RESISTOR VALUES ARE IN OHMS Ω, ± 5% ¼ WATT.
3. NOTICE TO BE GIVEN ON ANY PART CHANGES.
4. P.C. BOARD NO. 113-3004-103.
5. COMPONENTS R1 & R25 ARE ZERO Ω JUMPERS.
Q2
R2
R4 360K
R7 220K
R12 360K
C9 .15
Q1
C5 10PF
C1
C16 15
R29 10K
R15 200K
C8 .33
C10 .001
R24 300K
C4 15
R9 20K
R13 200K
A1
(LM301)
C7 10PF
CR1
+15V
15V
R27 130K
R30 50K TRIM
C15 1μF
1.8V
R23 47K
R19 47K
30K
C12 47
TOP VIEW
RECT. CAP 1
RECT. IN 1
CELL IN 1
GND
INV. IN 1
RES. R3 1
OUT 1
THD TRIM 1
RECT. CAP 2
RECT. IN 2
ΔG CELL IN 2
VGC
INV. IN 2
RES. R3 2
OUT 2
THD TRIM 2
NE 571 B
ANALOG COMPANDER
R3 39K
R6 10K
C3 .47
Q3
R11 4.7K
C6 15
R14 47K
R17 24K
Q6
R21 10K
Q7
R26 1K
C11 .001
50K TRIM
R18
R28 100K
C14 .68
R20 68K
C13 .47
R22 10K
C17 .15
R16 360K
R10 270K
R8 360K
Q5
Q4
R5 39K
10K
C2 1μF
MKR INNOVATIONS INC.
T. BARNHART
SCHEMATIC DIAGRAM - COMPANDER
DIGITAL DELAY
4-17-78
113-4004-103



M	L	F CUTOFF	PINS SELECTED X	Y
1	1	20K HZ	11	4 (5)
1	0	10K HZ	15	2 (2)
0	1	5K HZ	14	3 (1)
0	0	2.5K HZ	12	1 (0)

X - PIN 13
Y - PIN 3

PINS 9 (VSS) AND 6 (INH.) TO GND.

J9-11,12

M J9-2 → TO PIN 9 ON ALL 4052'S

F SELECT
L J9-1 → TO PIN 10 ON ALL 4052'S

+15V J9-15 → TO PIN 8 ON ALL 4558'S

-15V J9-16 → TO PIN 4 ON ALL 4558'S

+7.5V J9-13 → TO PIN 16 ON ALL 4052'S

-7.5V J9-14 → TO PIN 7 ON ALL 4052'S

J9-3,4,7,10 - NO CONNECTION

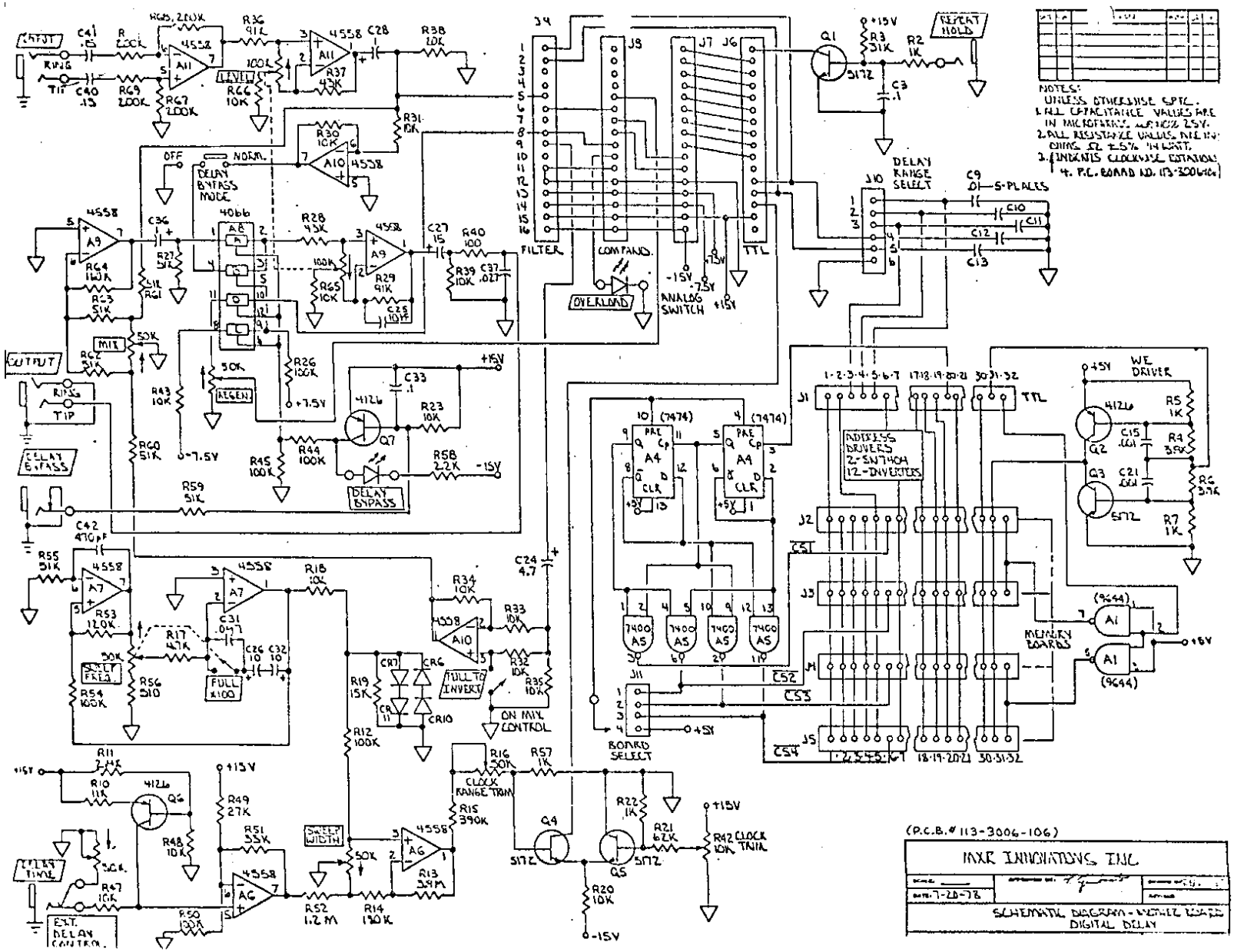
(P.C.B. # 113-3005-103

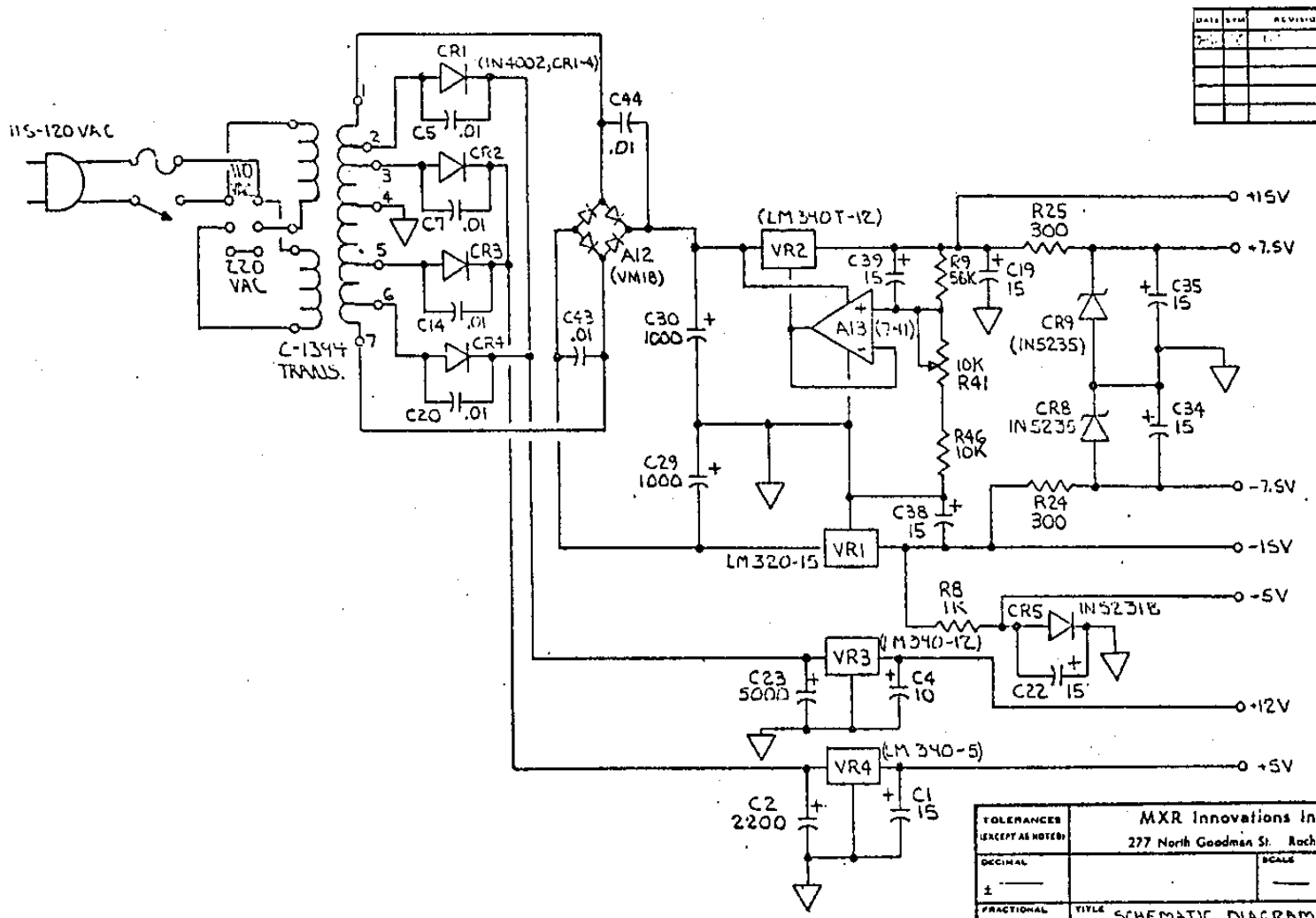
MXR INNOVATIONS INC.

SCALE:	APPROVED BY:	DRAWN BY:
DATE: 8-1-78		

SCHEMATIC DIAGRAM - FILTER BOARD - DIGITAL DELAY

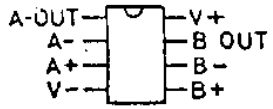
DRAWING NUMBER 113-4005-101


INPUT
OUTPUT
RING
TIP
DELAY BYPASS
DELAY BYPASS MODE
OFF
NORM.
LEVEL
REGEN
MIX
FEEDBACK
FULL ×100
FULL TO INVERT
ON MIX CONTROL
CLOCK RANGE TRIM
CLOCK TRIM
SWEEP WIDTH
SWEEP FREQ
DELAY TIME
EXT. DELAY CONTROL
FILTER
COMPAND.
OVERLOAD
ANALOG SWITCH
REPEAT HOLD
DELAY RANGE SELECT
BOARD SELECT
INDEXING DRIVERS 2-SN74OH 12-INVERTERS
WE DRIVER
MEMORY BOARDS
TTL
NOTES:
UNLESS OTHERWISE SPEC.
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS UNLESS 25V.
2. ALL RESISTANCE VALUES ARE IN OHMS Ω ±5% ¼ WATT.
3. (INDICATES CLOCKWISE ROTATION
4. P.C. BOARD NO. 113-3006-106
(P.C.B.# 113-3006-106)
MXR INNOVATIONS, INC.
7-20-78
SCHEMATIC DIAGRAM - MEMORY BOARD
DIGITAL DELAY



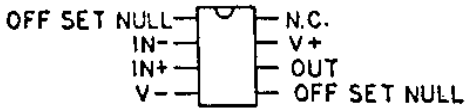
TOLERANCES (EXCEPT AS NOTED)	MXR Innovations Incorporated 277 North Goodman St. Rochester, N.Y. 14607		
DECIMAL ±		SCALE —	DRAWN BY
FRACTIONAL ±	TITLE SCHEMATIC DIAGRAM - POWER SUPPLY DIGITAL DELAY		
ANGULAR ±	DATE 3-18-77	DRAWING NUMBER 113-4006-103 PAGE 2	

4558
TOP VIEW



DUAL OP-AMP

741
TOP VIEW

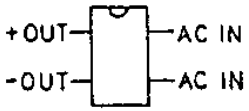


OP-AMP

2N5172
2N4126
FLAT DOWN · TOP VIEW

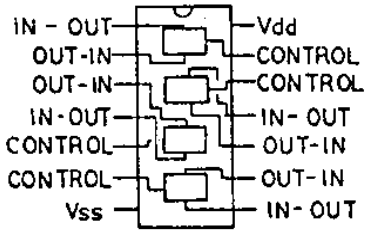
TRANSISTORS

VM-18
TOP VIEW



BRIDGE RECTIFIER

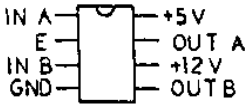
CD 4066 B
TOP VIEW



CMOS
QUAD BILATERAL
SWITCH

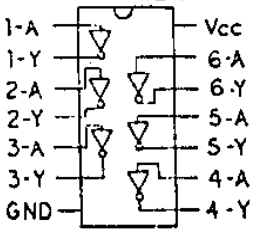
CONTROL	SWITCH
0	OFF
1	ON

5644
TOP VIEW



DUAL TTL TO
MOS DRIVER

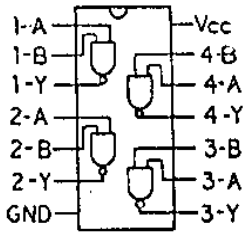
SN 7404 N
TOP VIEW



HEX INVERTER

POSITIVE LOGIC
$Y = \bar{A}$

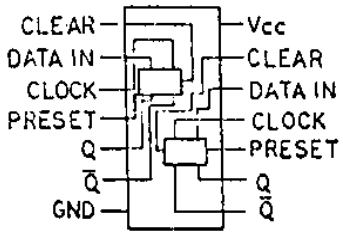
SN 7400 N
TOP VIEW



QUAD 2 INPUT
POSITIVE NAND GATE

POSITIVE LOGIC
$Y = \overline{AB}$

SN7474N
TOP VIEW



DUAL D TYPE
POSITIVE EDGE TRIGGERED
FLIP-FLOP W/ PRESET & CLEAR.

PRESET	CLEAR	CLOCK	D	OUT Q	OUT $\bar{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_o	$\bar{Q}_o$

*NOTE: THIS CONFIGURATION IS NONSTABLE. IT WILL NOT PERSIST WHEN PRESET AND CLEAR INPUTS RETURN TO THEIR INACTIVE (HIGH) LEVEL.

REVISION LOG

LEVEL	DATE	REMARKS	AUTH.	DRN.	CHK.

MXR Innovations Inc.

TOLERANCE:	DATE: 10-16-79	PRINT DATE:	DRAWN BY: B. Kelley
DECIMAL: —	SCALE: —		APPROVED BY: S.S. 10/4/79
FRACTIONAL: —	TITLE: COMPONENT PIN OUT SCHEMATIC MOTHER BOARD DDL PAGE 3 OF 3		
ANGULAR: —	DRAWING NUMBER: 113 4006		REVISION LEVEL: 103